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WiMax PLL's FIR Filter Design Using LMIs

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Abstract—WiMax technology evolved greatly over the last decade. Using optimization techniques to improve the behavior of filters in phase-locked loop (PLL) in terms of overshoot and setlling time is a challenging task. This paper introduces a new PLL's loop filter design methodology that meets mobile WiMax design objectives such as small settling time, minimum overshoot and working mobile WiMax frequency range. LMI optimization based on semidefinite programmimg is used for FIR filter design to optimize conflicting objectives. The obtained results are compared with linear programming results. The LMI results outperformed results of linear programming and other comparable designs.

Index Terms— LMI, PLL, FIR, Mobile WiMax, Frequency Synthesizer

1. Introduction

The fourth generation (4G) of mobile broadband networks is based on the foundation of worldwide Interoperability for Microwave Access (WiMax)[1]. Quality of Service (QoS) for different traffic classes, robust security, and mobility are guaranteed by WiMax. The phase-locked loop (PLL) is basically an electronic circuit that maintains a constant phase angle relative to a reference signal by controlling an oscillator [2]; moreover, it plays a significant part in WiMax system. PLLs are most commonly used in frequency synthesizers of wireless systems. A frequency synthesizer generates a range of output frequencies from a single stable reference frequency of a crystal oscillator [3]. In communication systems, many applications require a range of frequencies or a multiplication of a periodic signal. For example, in most FM radios, a PLL frequency synthesizer is used to generate 101 different frequencies. In order to generate highly accurate frequencies with varying precisely steps, such as from 600 MHz to 800 MHz in steps of 200 KHz, most wireless transceiver designs employ a frequency synthesizer. Frequency Synthesizers are also widely used in signal generators and in instrumentation systems, such as spectrum analyzers and modulation analyzers. A basic configuration of a frequency synthesizer is shown in Figure 1.

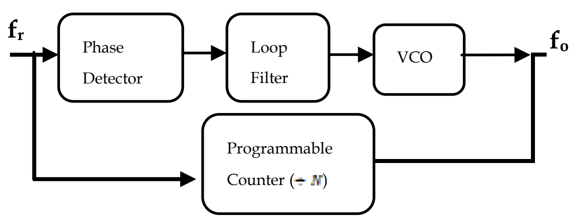

Fig. 1. Basic Frequency Synthesizer

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The basic frequency synthesizer includes a very stable crystal oscillator and N- programmable divider in the feedback loop in addition to the PLL. The programmable divider divides the output of the Voltage Controlled Oscillator (VCO) by N and locks to the reference frequency generated by a crystal oscillator.

The output frequency of VCO is a function of the control voltage generated by the phase detector/comparator (PD). The output of the phase comparator, is proportional to the phase difference between the signals applied at its two inputs, controls the frequency of the VCO. Thus, the phase comparator input from the VCO through the programmable divider remains in phase with the reference input of crystal oscillator. Therefore, the VCO frequency is maintained at Nf_r. This relation can be expressed as

$$f_r = \frac{f_0}{N} \qquad (1)$$

where f_r is fractional frequency and N is an integer number.

This implies that the output frequency, f_0 is equal to

$$f_0 = Nf_r \qquad (2)$$

Using this technique, a number of frequencies separated by f_r and a multiple of N can be produced. For example, if the input frequency is 24 KHz and the N is 32, then the output frequency is 0.768MHz. In the same manner, if N is an array of numbers, then the output frequencies will be a proportional array. This basic technique form using phase locked loop technique is used to develop a frequency synthesizer using a single reference frequency. As for the phase detector in Figure 1, $\theta_i(s)$ represents the phase input, $\theta_e(s)$ the phase error, and $\theta_0(s)$ output phase. Phase error (phase detector output) can be calculated such as

$$\theta_e(s) = \frac{1}{1+G(s)H(s)}\theta_i(s) \qquad (3)$$

and the VCO output can be calculated such as

$$\theta_0(s) = \frac{G(s)}{1+G(s)H(s)}\theta_i(s) \qquad (4)$$

where $G(s)$ is the feedforward transfer functions, and $H(s)$ is the feedback transfer functions [3].

The loop filter performs the filtering operation of the error voltage (coming out from the Phase Detector). The output of phase detector consists of a dc component superimposed on an ac component. The ac part is an undesired input signal to the VCO; hence, a low pass filter is used to filter out the ac component. The loop filter is an essentional functional block in determining the performance of the loop. In addition, a loop filter introduces poles to the PLL transfer function, which plays key role in determining the bandwidth of the PLL. Since higher order loop filters offer better noise cancelation, a loop filter of order 2 or more is used in most of the critical application PLL circuits.

One desirable property of all PLLs is that the reference and feedback clock edges be brought into very close alignment [4]. The average difference in time between the phases of the two signals when the PLL has achieved lock is called the static phase offset (the steady-state phase error). The variance between these phases is called tracking jitter. Ideally, the static phase offset should be zero, and the tracking jitter should be as low as possible.

Phase noise is another type of jitter observed in PLLs [4], and is caused by the oscillator itself and by elements used in the oscillator's frequency control circuit. To keep phase noise low in PLL circuits, it is best to avoid saturating logic families such as transistor-transistor logic (TTL) or CMOS.

The main contribution of this paper is designing a specified PLL loop filter that works properly and efficiently with Mobile WiMax system. Selecting the filter's coefficients is based on LMIs using semidefinite programming (SDP) optimization techniques that are compatible with Mobile WiMax system. The designed loop filter must be stable and meet the following specifications: Frequency range (2.3 – 2.7) GHz used for Mobile WiMax systems, small settling time to lower the lock-in range and a very small overshoot.

Traditional frequency synthesizers use low-pass analog filter to eliminate the high frequency components, but in this paper we use FIR digital low-pass filter to eliminate the high frequency components in order to improve noise immunity. N-Fractional Synthesizer is used instead of N-Integer Synthesizer to reduce noise resulted from the factor N.

This paper is organized as follows: Section 2 covers methodology used to design and optimize PLL loop filter. FIR low-pass digital filter using LP and LMI methods is introduced in section 3. Section 4 shows the results and discussions of LP and LMI designs. Conclusion and future work are outlined in section 5.

2. Methodology

The fractional-N PLL block diagram shown in Figure 2 consists of:

- Phase/Frequency detector which is assumed XOR type.
- Loop Filter which is the objective of our design which is a Low-pass filter (LPF).
- Voltage Control Oscillator (VCO).

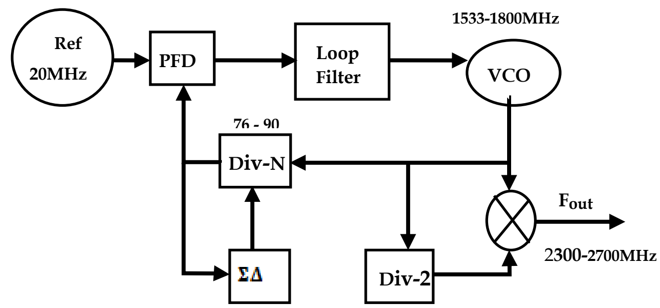

Fig. 2. Fractional-N PLL block diagram

We started by designing an Integer-N PLL: 125 KHz reference pushes N from 18400 to 21600 (2700/.125). The resulted loop filter cutoff (<12.5 KHz) produced big settling time and the VCO phase noise increased by $20\log_{10}(N) \approx 87$dB.

To overcome the previous drawback, we used Multi-Modulus Fractional PLL with the following specifications:

- Fractional value between N and 2N-1 (64-127).
- Sigma Delta Modulator (Programmable resolution).
- Large Reference (20MHz) for good tradeoff with settling time.
- Reduced N impact on phase noise by 45dB over Integer N.

Example 1: To obtain 2300MHz frequency, we produced 1533MHz (from VCO) and then upconvert it to 2300MHz (1533MHz * 1.5 ≈ 2300MHz). The 1533MHz can be produced with N = 76 and a fraction = 0.65 (means that 20MHz * (76 + 0.65) = 1533MHz).

As a result, for N = (76 ~ 90), it can produce frequency range (1533MHz ~ 1800MHz), which can be upconverted to (2300MHz ~ 2700MHz).

Figure 2 shows the Fractional-N PLL design block diagram, with N range from 76 to 90 and $\Sigma\Delta$ is the fraction. Our goal now is to design digital FIR low pass loop filter in order to meet the previously mentioned requirements. The design will be encouraged by two different optimization methods, Linear programming (LP) and Semi-Definite programming (SDP).

3. FIR Low-Pass Filter Design

We consider the problem of designing a finite impulse response (FIR) filter with upper and lower bounds on its frequency response magnitude [5]: given filter length N, find filter tap coefficients $h \in R^N,\ h = \big(h(0), \ldots, h(N-1)\big)$, such that the frequency response $H(\omega) = \sum_{i=0}^{N-1} h(n)e^{-j\omega n}$ satifies the magnitude bounds

$$L(\omega) \le |H(\omega)| \le U(w), \quad \omega \in \Omega \subseteq [0,\pi] \tag{5}$$

over the frequency range Ω of interest.

One conventional approach to FIR filter design is Chebychev approximation of a desired filter response $D(\omega)$, i.e., one minimizes the maximum approximation error over Ω.

We present a new way of solving the proposed class of FIR filter design problems, based on magnitude design i.e., instead of designing the frequency response $H(\omega)$ of the filter directly, we design its power spectrum $|H(\omega)|^2$ to satisfy the magnitude bounds [5].

Let autocorrelation function $r(n)$ denote

$$r(n) = \sum_{k=-\infty}^{\infty} h(k)h(k+n) \quad (6)$$

where we take $h(k) = 0 \ for \ k < 0 \ or \ k > N-1$. The sequence $r(n)$ is symmetric around $n = 0, zero \ for \ n \le -N \ or \ n \ge N, and \ r(0) \ge 0$. Note that the Fourier transform of $r(n)$,

$$R(\omega) = \sum_{n=-\infty}^{\infty} r(n)e^{-j\omega n} = |H(\omega)|^2 \quad (7)$$

is the power spectrum of $h(n)$. If we use r as our design variables, we can reformulate the FIR design problem in RN as

$$\begin{aligned} &find \quad r = (r(0), \ldots\ldots, r(N-1)) \\ &Subject\ to \quad L^2(\omega) \le R(\omega) \le U^2(\omega), \quad \omega \in \Omega \qquad (8) \\ &R(\omega) \ge 0, \quad \omega \in [0,\pi] \end{aligned}$$

The non-negativity constraint $R(\omega) \ge 0$ is a necessary and sufficient condition for the existence of x satisfying (6) by the Fejér-Riesz theorem (see § 4 in [5]). Once a solution of (7) is found, an FIR filter can be obtained via spectral factorization. An efficient method of minimum-phase spectral factorization is given in Section 4 in [5].

3.1 LP formulation

A common practice of relaxing the semi-definite program (7) is to solve a discretized version of it, i.e., impose the constraints only on a finite subset of the [0,π] interval and the problem becomes

$$\begin{aligned} &find \quad r = (r(0), \ldots\ldots, r(N-1)) \\ &Subject\ to \quad L^2(\omega_i) \le R(\omega_i) \le U^2(\omega_i), \quad \omega_i \in \Omega \qquad (9) \\ &R(\omega_i) \ge 0, \quad i = 1, \ldots\ldots, M, \end{aligned}$$

where $0 \le \omega_1 < \omega_2 < \cdots < \omega_M \le \pi$. Since $R(\omega_i)$ is a linear function in r for each i, (8) is in fact a linear programming problem that can be efficiently solved. When M is sufficiently large, the LP formulation gives very good approximations of (7). A rule of thumb of choosing M, $M \approx 15N$, is recommended in [6]. According to that we assumed M = 15N along this paper.

3.2 LMI formulation

We will show that the non-negativity of $R(\omega_i)$ for all $\omega \in [0,\pi]$ can be cast as an LMI [7] constraint and imposed exactly at the cost of $N(N-1)/2$ auxiliary variables. We will use the following theorem.

Theorem 1 *Given a discrete-time linear system* (A,B,C,D), *A stable,* (A,B,C) *minimal and* $D + D^T \ge 0$. *The transfer function* $H(z) = C(zI - A)^{-1}B + D$ *satisfies*

$$H(e^{j\omega}) + H^*(e^{j\omega}) \ge 0 \quad for\ all \quad \omega \in [0,2\pi] \qquad (10)$$

if and only if there exists real symmetric matrix P such that the matrix inequality

$$\begin{bmatrix} P - A^T PA & C^T - A^T PB \\ C - B^T PA & D + D^T - B^T PB \end{bmatrix} \ge 0. \qquad (11)$$

is satisfied. Detailed proof of this theorem can be found in [5].

In order to apply Theorem 1, we would like to define H(z) as deadbeat system where H(z) is defined as a rational function with its denumerator consists of one term with z to the power of N. Then, this system is represented in delay mode, z-1, which leads to a polynomial with N coefficients stored in array r. Thus,

(A,B,C,D) is defined such as

$$H(z) = C(zI - A)^{-1}B + D = \frac{1}{2}r(0) + r(1)z^{-1} + \cdots + r(N-1)z^{-(N-1)} \qquad (12)$$

An obvious choice is the controllability canonical form:

$$A = \begin{bmatrix} 0 & 0 & & \cdots & 0 \\ 1 & 0 & & \cdots & 0 \\ & 1 & & & \\ \vdots & & \ddots & \ddots & \vdots \\ 0 & & & 1 & 0 \end{bmatrix}, B = \begin{bmatrix} 1 \\ 0 \\ \vdots \\ 0 \end{bmatrix},$$

$$C = [r(1) \quad r(2) \quad \cdots \quad r(N-1)], \quad D = \frac{1}{2}r(0) \qquad (13)$$

It can be easily checked that (A,B,C,D) given by (11) satisfies (10) and all the hypotheses of Theorem 1. Therefore the existence of r and symmetric P that satisfy the matrix inequality (9) is the necessary and sufficient condition for $R(\omega) \ge 0,\ for\ all\ \omega \in [0,\pi]$ by Theorem 1.

Note that (9) depends affinely on r and P. Thus we can formulate the SDP feasibility problem:

$$find \qquad r \in R^N \ and \ P = P^T \in R^{N-1 \times N-1}$$

$$\textit{Subject to} \quad L^2(\omega_i) \le R(\omega_i) \le U^2(\omega_i),\ \omega_i \in \Omega \qquad (14)$$

$$\begin{bmatrix} P - A^T P A & C^T - A^T P B \\ C - B^T P A & D + D^T - B^T P B \end{bmatrix} \ge 0$$

with (A, B, C, D) given by (11). The SDP feasibility problem (12) can be cast as an ordinary SDP and solved efficiently.

4. Results and Discussions

In order to perform simulation for the designed filters, a simulation module as shown in Figure 3 is built using MATLAB and Simulink.

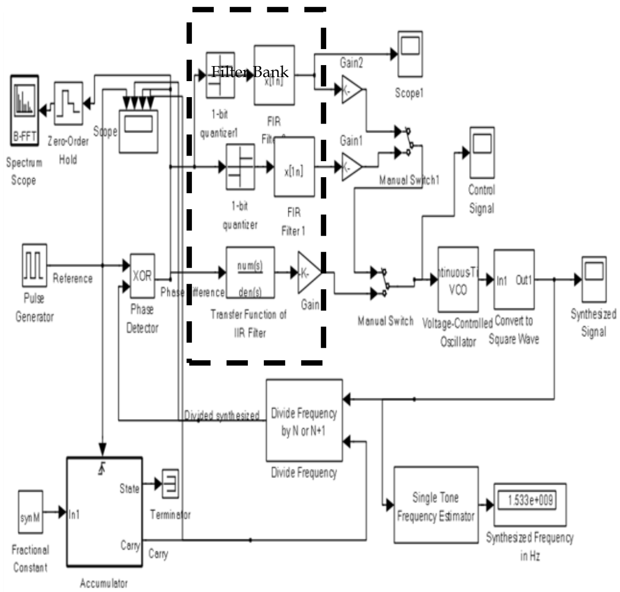

Fig. 2. PLL Frequency Synthesizer Simulation Model

The FIR filters parameters are obtained using the MATLAB convex optimization toolbox, CVX [8]. The simulation module consists of:

- Reference Frequency: Pulse generator is chosen to produce 20MHz.
- Filter Bank: two filters are designed and separated by manual switch as shown in Figure 3.
- Voltage Controlled Oscillator (VCO) with output signal amplitude equal to 1V, quiescent frequency equal to 1.511 GHz, and input sensitivity equal to 10MHz/V.
- Phase Detector: XOR type selected.
- Frequency Divider which produces (synN + synM) values used to divide the output of VCO. Where synN is the integer and synM is the fraction.
- Sigma/Delta Modulator: to produce the required fraction synM.
- The Gain formula $K = K_x * \frac{(synFr*synN - synFq)}{synSen}$, where $K_x = 2.5$ after the output of FIR filter.

The simulation model produced synthesized frequency in the range of (1.533GHz – 1.8GHz) that must be multiplied by 1.5 to obtain the required range (2.3GHz – 2.7GHz).

4.1 LP (Linear programming)

The FIR filter design is obtained using LP as shown in Figure 4.

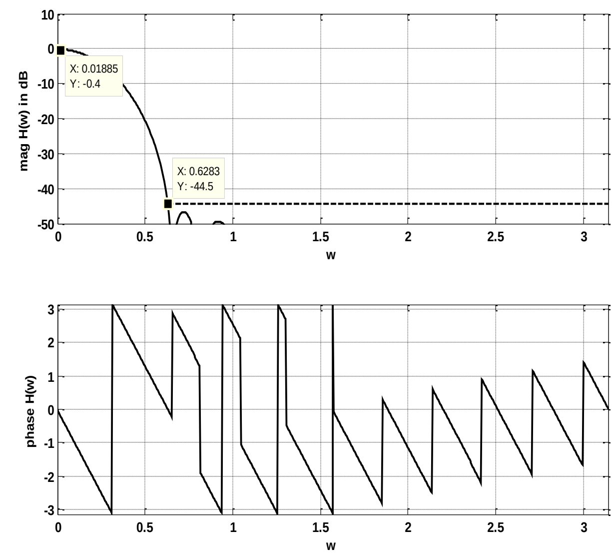

Fig. 3. Magnitude/Phase Response (LP)

Figure 4 shows the designed FIR filter length of 21 taps where filter order equals to 20. Figure 4 shows that:

- The maximum passband ripple does not exceed 0.4 dB with $w_{pass} = 0.01885 = 0.006\pi\ rad/s$.
- Stopband attenuation is below -44.5 dB with $w_{stop} = 0.6283 = 0.2\pi\ rad/s$.

The simulation results of the Mobile WiMax for this FIR filter produced the correct and proper output frequency as shown in Figure 3. The simulation result of the control signal using this FIR filter as shown in Figure 5 produced: zero overshoot, rise time of $0.2749\mu s$, and settling time of $0.5498\mu s$.

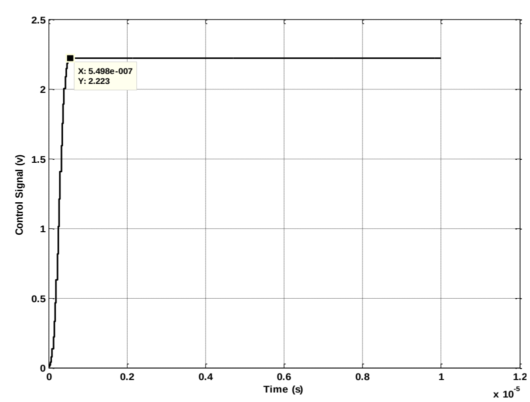

Fig. 4. Control Signal of VCO input using Designed FIR Filter

4.2 LMI

The second FIR filter design is obtained using SDP as shown in Figure 6.

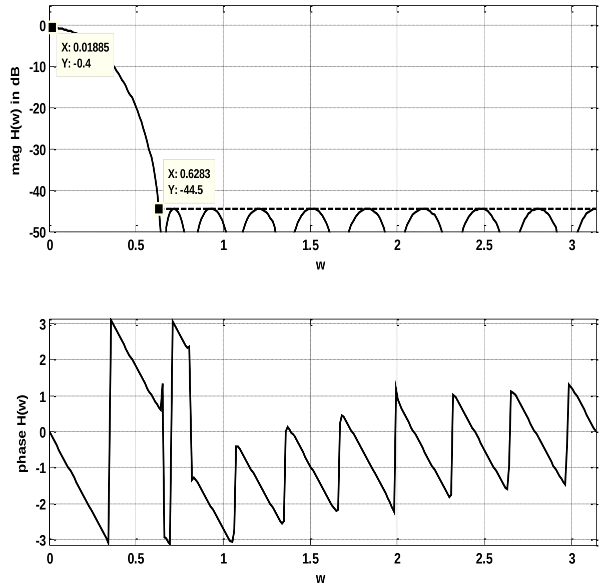

Fig. 5. FIR Filter Magnitude/Phase Response (SDP)

Figure 6 shows a 19 taps FIR filter with filter order of 18 (fewer than LP FIR length). Figure 6 shows that:

- The maximum passband ripple does not exceed 0.4 dB with $w_{pass} = 0.01885 = 0.006\pi\, rad/s$.
- Stopband attenuation is below -44.5 dB with $w_{stop} = 0.6283 = 0.2\pi\, rad/s$.

The simulation results of Mobile WiMax as shown in Figure 3 worked properly and produced the correct output frequency. The simulation results of the control signal using this FIR filter as shown in Figure 7 produced: zero overshoot, rise time of 0.25μs, and settling time of 0.4998μs.

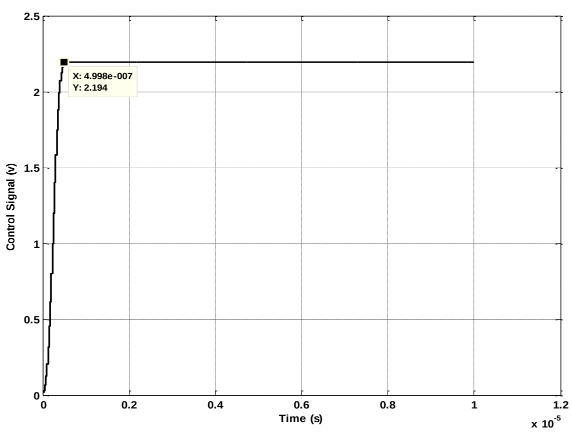

Fig.7. Control Signal of VCO input using Designed FIR Filter (SDP)

The filter design using SDP technique outperformed LP technique with reduced filter length of 19 taps instead of 21 taps, lower settling time and lower rise time. Moreover, the proposed SDP filter design also outperformed filter designs by Chou's [9], Staggs' [10] and Kozak's [11] in terms of settling time and overshoot as shown in Table 1. Unfortunately, the rise time did not meet Chou's and Staggs' results. Filter design using SDP outperformed other techniques regarding filter order, settling time and overshoot.

TABLE 1
COMPARISON BETWEEN PROPOSED FIR DIGITAL FILTER DESIGNS AND OTHER DESIGNS

	FIR filter design (LP)	FIR filter design (SDP)	Chou's	Staggs'	Kozak's
Settling time	0.5498 μs	0.4998 μs	40 μs	40 μs	≈ 10μs
Rise time	≈ 0.2749 μs	≈ 0.25 μs	≈ 0.07313 μs	≈ 0.1μs	≈ 1μs
Overshoot	Zero	zero	≈ 21%	≈ 25%	≈ 29.6%

5. CONCLUSION AND FUTURE WORK

Optimal design of phase-locked loop in WiMax technology can improve system behavior (overshoot & settling time). A new loop filter design method for frequency synthesizer is used in mobile WiMax. The proposed method took into consideration various design objectives such as: small settling time, minimum overshoot and mobile WiMax frequency range. FIR digital low pass filter was designed using linear programming and LMI optimization based on semidefinite programming. Simulations results showed that FIR lowpass digital filter utilizing linear programming and semidefinite programming improved the transient behavior. The simulated results also showed that the filter met the Mobile WiMax systems working frequency range of (2.300 GHz – 2.700 GHz) and has the power to include much higher frequency bands. The designed method of LMI optimization using Semidefinite programming outperformed the LP filter design and did much better than similar work by others.
Further research can concentrate more on VCO noise and optimizing filter order.

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